What is claimed is:

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1. An apparatus comprising:

a memory device having a memory device input data bus including a least significant bit and a plurality of non-least significant bits; and

a first repair router having a first repair router input data bus including a least significant bit and a plurality of non-least significant bits, and a first repair router output data bus coupled to the memory device input data bus, the first repair router having internal routing circuitry to route any of the plurality of non-least significant bits of the first repair router input data bus to the least significant bit of the memory device input data bus.

2. The apparatus of claim 1 wherein:

the plurality of non-least significant bits includes a next-to-least significant bit; and

the first repair router further includes additional repair routing circuitry to route any of the non-least significant bits to the next-to-least significant bit.

3. The apparatus of claim 1 wherein the memory device includes a memory device output data bus including a least significant bit and a plurality of non-least significant bits, the apparatus further comprising:

a second repair router having a second repair router input data bus coupled to the memory device output data bus, and having a second repair router output data bus including a least significant bit and a plurality of non-least significant bits, the second repair router having internal routing circuitry to route the least significant bit of the memory device output data bus to any of the plurality of non-least significant bits of the second repair router output data bus.

4. The apparatus of claim 3 wherein the memory device includes a plurality of address ranges, and the first and second repair routers include address decoding circuitry to decode each of the plurality of address ranges.

5. The apparatus of claim 4 wherein the memory device includes two address ranges defined by a state of a most significant address bit.

6. The apparatus of claim 3 further comprising a display device coupled to the second repair router output data bus.

7. The apparatus of claim 6 wherein the display device is a color display device, and the memory device and first and second repair routers influence a first color of the color display device, the apparatus further comprising:

a second memory device; and

a second pair of repair routers coupled to the second memory device to influence a second color of the color liquid crystal display.

8. The apparatus of claim 7 further comprising:

a third memory device; and

a third pair of repair routers coupled to the third memory device to influence a third color of the color liquid crystal display.

9. A memory device comprising:

a plurality of addressable memory locations, each including a least significant bit and a plurality of non-least significant bits; and

a first repair router having a repair router input data bus with a least significant bit and a plurality of non-least significant bits, and having a repair router output data bus coupled to the plurality of addressable memory locations, the first repair router including routing circuitry to route any of the plurality of non-least

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significant bits of the repair router input data bus to the least significant bit of at least one of the plurality of addressable memory locations.

10. The memory device of claim 9 wherein:

the plurality of addressable memory locations are arranged into a plurality of address ranges; and

the first repair router further includes address decoding circuitry to decode each of the plurality of address ranges.

11. The memory device of claim 10 further comprising a second repair router coupled to an output data bus of the memory device, the second repair router including routing circuitry to reverse any routing performed by the first repair router.

12. The memory device of claim 9 wherein the first repair router is configured to route a specific non-least significant bit to the least significant bit of the plurality of addressable memory locations when a problem exists with the specific non-least significant bit in at least one of the plurality of addressable memory locations.

13. The memory device of claim 9 further comprising a second repair router coupled to an output data bus of the memory device, the second repair router including routing circuitry to reverse any routing performed by the first repair router.

14. The memory device of claim 9 wherein:

the plurality of non-least significant bits includes a next-to-least significant bit; and

the first repair router further includes routing circuitry to route any of the plurality of non-least significant bits of the repair router input data bus to the next-to-least significant bit of at least one of the plurality of addressable memory locations.

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15. A display system comprising:

a display device having an array of pixels;

a memory having a plurality of addresses, each of the plurality of addresses corresponding to one pixel in the array of pixels, and each of the plurality of addresses including a least significant data bit and a plurality of non-least significant data bits; and

a repair router to utilize the least significant bit of at least one of the plurality of addresses to hold non-least significant information.

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16. The display system of claim 15 wherein the display device is a silicon light modulator.

17. The display system of claim 15 wherein the memory is configured to hold a first color information, the display system further comprising:

a second memory configured to hold second color information; and

a second repair router coupled to the second memory.

18. The display system of claim 17 further comprising:

a third memory configured to hold third color information; and

a third repair router coupled to the third memory.

19. The display system of claim 15 wherein:

the plurality of addresses are arranged in a plurality of groups; and

the repair router includes routing circuitry to utilize the least significant bits of each of the plurality of groups separately.

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20. An integrated circuit comprising:

a memory device having an input data bus and an output data bus; and

first and second repair routers coupled to the input data bus and the output data bus, respectively, the first and second repair routers including routing circuitry

to route data to and from the memory device as a function of defects in the memory device.

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21. The integrated circuit of claim 20 further comprising a reflective electrode coupled to the memory, the reflective electrode having a plurality of pixels responsive to data from the memory device as received by the second repair router.

22. The integrated circuit of claim 21 wherein:

the memory device includes a plurality of groups of data locations; and

the first and second repair routers each include circuitry to separately route data for each of the plurality of groups of data locations.

23. The integrated circuit of claim 22 further comprising:

second and third memory devices; and

second and third pairs of repair routers coupled to the second and third memory devices respectively.